AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus, comprising:

a phase controller to generate interrelated control signals based upon a comparison of a recovered clock signal with a data signal, the phase controller having a plurality of voltage controllers each with its own charge storage circuitry to generate the interrelated control signals, respectively;

a phase-frequency detector coupled with said phase controller to sample data of the data signal at a sample rate based on the recovered clock signal and to output a comparison signal based on samples of the data;

phase update logic circuitry coupled with the phase-frequency detector to generate charge and discharge signals based upon the comparison signal, to act upon the charge storage circuitry of each of the voltage controllers; and

a phase interpolator coupled with said phase controller to change a phase of the recovered clock signal based upon a combination of amplitude contributions from more than one phase of a reference clock signal, wherein the amplitude contributions from the more than one phase are weighted in accordance with the interrelated control signals.

2. Canceled.

3. (Previously Presented) The apparatus of claim 1, wherein the phase-frequency detector comprises circuitry to compare at least a pre-data bit sample, a mid-data bit sample, and a post-data bit sample to determine the comparison signal.

Claims 4-5 (Canceled).

6. (Previously Presented) The apparatus of claim 1, wherein the phase update logic circuitry comprises circuitry to manage the distribution of phase updates to a phase control circuit of said phase controller, associated with a managing interrelated control signal of the interrelated control signals.

Claims 7-8 (Canceled).

9. (Previously Presented) An apparatus, comprising:

a phase controller to generate interrelated control signals based upon a comparison of a recovered clock signal with a data signal;

a phase interpolator coupled with said phase controller to change a phase of the recovered clock signal with an analog transition based upon a combination of amplitude contributions from more than one phase of a reference clock signal, wherein the amplitude contributions from the more than one phase are weighted in accordance with the interrelated control signals, wherein said phase controller comprises a first phase control circuit to generate a first interrelated control signal of the interrelated control signals and a second phase control circuit to generate a second interrelated control signal of the interrelated control signals, wherein the second interrelated control signal decreases in amplitude at substantially the same rate as the first interrelated control signal increases in amplitude to yield said analog transition in the phase of the recovered clock signal.

10. (Original) The apparatus of claim 9, wherein said phase controller further comprises:

charge circuitry to transition the amplitude of the first interrelated control signal higher in response to a charge signal; and

discharge circuitry to transition the amplitude of the second interrelated control signal lower in response to a discharge signal.

11. (Original) The apparatus of claim 10, wherein said phase controller further comprises:

trip high circuitry to compare the amplitude of the first interrelated control signal to a high amplitude reference; and

trip low circuitry to compare the amplitude of the second interrelated control signal to a low amplitude reference.

12. (Original) The apparatus of claim 1, wherein said phase controller comprises hysteresis circuitry to prevent chatter in an overflow signal.

13. (Previously Presented) An apparatus, comprising:

a phase controller to generate interrelated control signals based upon a comparison of a recovered clock signal with a data signal;

a phase interpolator coupled with said phase controller to change a phase of the recovered clock signal with an analog transition based upon a combination of amplitude contributions from more than one phase of a reference clock signal, wherein the amplitude contributions from the more than one phase are weighted in accordance with the interrelated control signals, wherein said phase controller further comprises common mode feedback circuitry coupled with more than one phase control circuit to substantially compensate for changes in a common mode amplitude of managing interrelated control signals of the interrelated control signals.

14. (Currently Amended) The apparatus of claim 1, wherein said phase interpolator comprises phase control circuitry to transition ~~the~~ a bias current, based upon the interrelated control signals, of a differential current-steering mechanism to adjust the amplitude contributions.

15. 6 (Original) The apparatus of claim 14, 5 wherein said phase interpolator comprises a degenerative mesh coupled with the phase control circuitry to degenerate a transfer characteristic of the phase control circuitry.

16. 7 (Original) The apparatus of claim 15, 6 wherein said phase interpolator further comprises circuitry to filter an output of the differential current-steering mechanism.

17. 12 (Currently Amended) A method, comprising:

receiving a data signal;

comparing the data signal to a recovered clock signal;

generating interrelated control signals based on said comparing; ~~and~~

generating, based upon said comparing, a charge signal to increase an amplitude of a first interrelated control signal of the interrelated control signals substantially simultaneously with generating a discharge signal to decrease an amplitude of a second interrelated control signal of the interrelated control signals; and

combining amplitude contributions from phases of a reference clock signal wherein the amplitude contributions are based on the interrelated control signals, to change a phase of the recovered clock signal ~~with an analog transition~~.

Claims 18-20 (Canceled).

21. 13 (Currently Amended) ~~The method of claim 17~~A method, comprising:

receiving a data signal;

comparing the data signal to a recovered clock signal;

generating interrelated control signals based on said comparing; and

combining amplitude contributions from phases of a reference clock signal wherein the amplitude contributions are based on the interrelated control signals, to change a phase of the recovered clock signal,

wherein said generating interrelated control signals comprises generating a first control signal and a second control signal to adjust the amplitude contributions from a first phase and a second phase of the phases of the reference clock signal, wherein adjustments to the amplitude contributions of the first phase and the second phase are substantially inversely proportional.

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~~22.~~ (Currently Amended) ~~The method of claim 17~~A method, comprising:

receiving a data signal;

comparing the data signal to a recovered clock signal;

generating interrelated control signals based on said comparing; and

combining amplitude contributions from phases of a reference clock signal wherein the amplitude contributions are based on the interrelated control signals, to change a phase of the recovered clock signal, wherein said generating interrelated control signals comprises generating a first ramping control signal and a second ramping control signal, wherein an amplitude of the first ramping control signal increases at a rate substantially equivalent to a rate that an amplitude of the second ramping control signal decreases.

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~~23.~~ (Currently Amended) ~~The method of claim 17~~A method, comprising:

receiving a data signal;

comparing the data signal to a recovered clock signal;

generating interrelated control signals based on said comparing; and

combining amplitude contributions from phases of a reference clock signal wherein the amplitude contributions are based on the interrelated control signals, to change a phase of the recovered clock signal, wherein said combining comprises:

generating differential signals with at least one of the phases of the reference clock signal, based upon the interrelated control signals; and

filtering the differential signals to change the phase of the recovered clock signal with the analog transition.

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24. (Currently Amended) The method of claim 23, wherein the filtering comprises integrating the differential signals.

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25. (Currently Amended) A system, comprising:

a front-end receiver to amplify a data signal;

a phase-frequency detector coupled with said front-end receiver to sample data from the data signal based upon a recovered clock signal and generate a comparison signal based on the sampled data;

phase update logic circuitry coupled with said phase-frequency detector to generate a signal based upon the comparison signal, to update a plurality of interrelated control signals;

a phase controller coupled with said phase update logic circuitry to generate the plurality of interrelated control signals based upon the comparison signal wherein said phase controller comprises a first phase control circuit to generate a first interrelated control signal of the interrelated control signals and a second phase control circuit to generate a second interrelated control signal of the interrelated control signals, wherein the second interrelated control signal decreases in amplitude at substantially the same rate as the first interrelated control signal increases in amplitude; and

a phase interpolator coupled with said phase controller to change a phase of the recovered clock signal with an analog transition based upon a combination of amplitude contributions from more than one phase of a reference clock signal, wherein the amplitude

contributions from the more than one phase are weighted in accordance with the interrelated control signals.

26. (Canceled).

27. (Original) The system of claim 25, wherein said phase interpolator comprises phase control circuitry to transition the bias current of a differential current-steering mechanism based upon the interrelated control signals.

Claims 28-30 (Canceled).